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6500/1 ONE-CHIP MICROCOMPUTER

INTRODUCTION

The MOS Technology 6500/1 is a complete, high-performance 8-bit NMOS microcomputer on a single chip, and is totally upward/downward software compatible with all members of the 6500 family.

The 6500/1 consists of a 6502 CPU, an internal clock oscillator, 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and flexible interface circuitry. The interface circuitry includes a 16-bit programmable counter/latch with four operating modes, 32 bidirectional input/output lines (including two edge-sensitive lines), five interrupts and a counter I/O line.

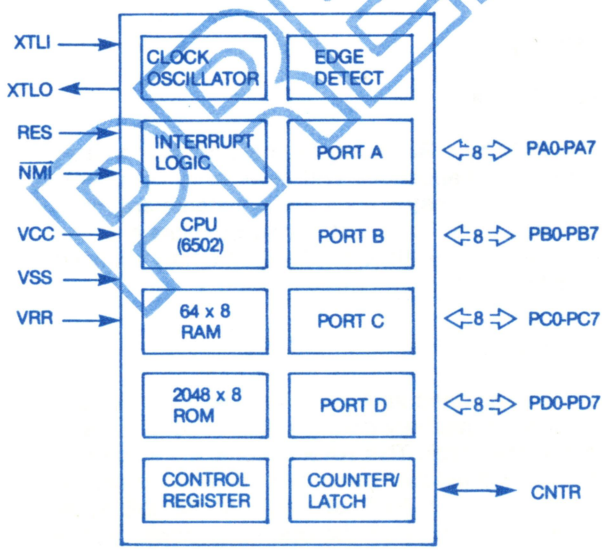
PRODUCT SUPPORT

To allow prototype circuit development, Mos Technology offers a PROM compatible 64-pin Emulator device. This device provides all 6500/1 interface lines plus routing the address bus, data bus, and associated control lines off the chip to be connected to external memory.

ORDERING INFORMATION

Order Number	Package Type	Frequency Option	Temperature Range
MPS6500/1	Plastic	1 MHz	0°C to 70°C
MCS6500/1	Ceramic	1 MHz	0°C to 70°C
MPS6500/1A	Plastic	2 MHz	0°C to 70°C
MCS6500/1A	Ceramic	2 MHz	0°C to 70°C
MCS6500/1E	Emulator Device 1MHz		
MCS6500/1EA	Emulator Device 2MHz		

Note: The RC frequency option is available only in the 1 MHz 6500/1.



Interface Diagram

FEATURES

- 6502 CPU
  - —Software upward/downward compatibility
  - —Decimal or binary arithmetic modes
  - —13 addressing modes
  - —True direct and indirect indexing
  - —Memory addressable I/O
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes
  - —Interval Timer —Event Counter
  - —Pulse Generator —Pulse Width Measurement
- Five Interrupts
  - —Reset —Two external edge sensitive
  - —Non-maskable —Counter
- 1 of 3 frequency references
  - —Crystal —Clock —RC (resistor only)
- 4 MHz max crystal or clock external frequency
- 2 MHz or 1 MHz internal clock
- 1 μs minimum instruction execution
- N-channel, silicon gate, depletion load technology
- Single +5V power supply
- 500 mW operating power
- Separate power pin for RAM
- 40 pin DIP
- 64 pin PROM compatible Emulator device

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

Clock Oscillator

The Clock Oscillator provides the basic timing signals used by the 6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 (∅2) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option (±35%).

Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. Each data transfer which takes place between the registers is caused by decoding the contents of both the Instruction Register and Timing Control Logic.

Program Counter

The 16-bit Program Counter provides the addresses which step the CPU through sequential instructions in a program. The Program Counter is incremented each time an instruction or data is fetched from memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter).

Accumulator

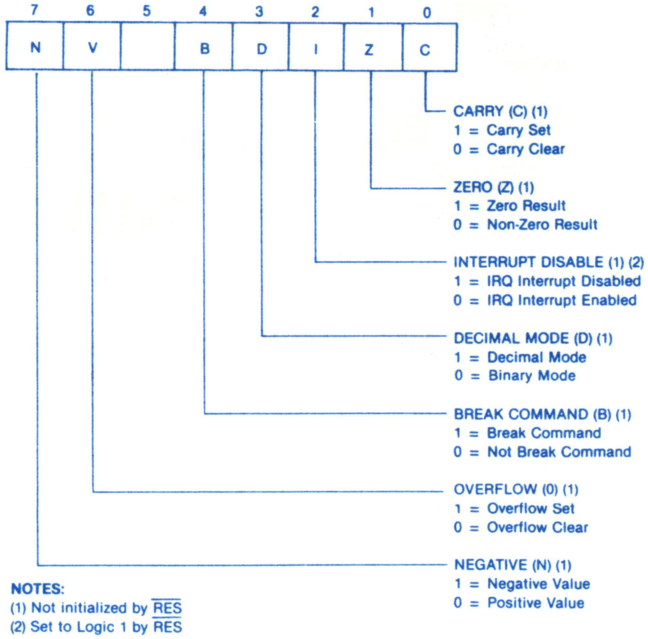
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers, X and Y. These registers can be used for general purpose storage, or as a displacement to modify the base address and thus obtain a new effective address. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation under direction of either the program or interrupts $\overline{NMI}$ and $\overline{IRQ}$. The stack allows simple implementation of nested subroutines and multiple level interrupts.



Processor Status Register

Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

MEMORY

2048 x 8 ROM

The 2048 byte Read-Only Memory (ROM) contains the program instructions and other fixed constants. These program instructions and constants are mask programmed into the ROM during fabrication of the 6500/1 device. The 6500/1 ROM is memory mapped from 800 to FFF.

64 x 8 RAM

The 64 byte Random Access Memory (RAM) is used for read/write memory during system operation, and contains the stack. This RAM is completely static in operation and requires no clock or dynamic refresh. A standby power pin, VRR, allows RAM memory to be maintained on 10% of the operating power in the event that VCC power is lost.

In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned memory addresses 0 to 03F.

INPUT/OUTPUT

Bidirectional I/O Ports

The 6500/1 provides four 8-bit input/output ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. See the system memory map for specific addresses. Each I/O line is individually selectable as an input or an output without line grouping or port association restrictions.

An internal active transistor drives each I/O line to the low state. An internal passive resistance pulls the I/O lines to the high state, eliminating the need for external pull-up resistors.

An option is available to delete the internal pull-up resistance on 8-bit port groups or on the CNTR line at mask time. This option is employed to permanently assign an 8-bit port group to input functions, to interface with CMOS drivers, or to interface with external pull-up devices.

Inputs

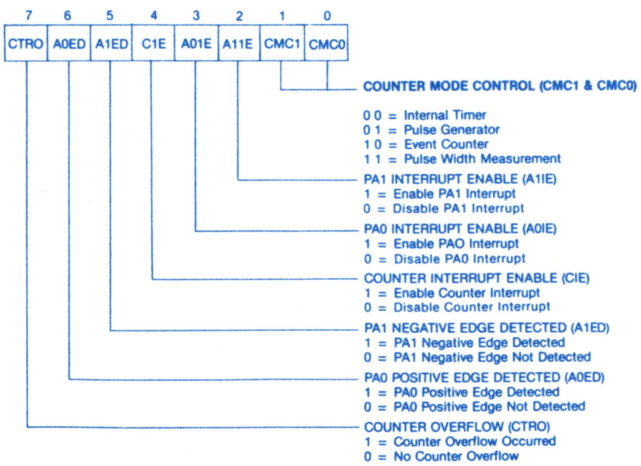
Inputs are enabled by setting the appropriate bit of the I/O port to the high state (Logic 1). A low input signal causes a logic 0 to be read. A high input signal causes a logic 1 to be read. $\overline{RES}$ loads Logic 1 into the I/O ports, thereby initializing all I/O lines as inputs.

Outputs

Outputs are set by loading the desired bit pattern into the corresponding I/O ports. A Logic 1 selects a high output; a Logic 0 selects a low output.

CONTROL REGISTER

The Control Register (CR) controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions. There are five control bits and three status bits. The control bits are set to Logic 1 or cleared to Logic 0 by writing the desired state into the respective bit positions. The Control Register is cleared to Logic 0 by the occurrence of $\overline{RES}$.



Control Register

EDGE DETECT CAPABILITY

There is an asynchronous edge detect capability on two of the Port A I/O lines. This capability exists in addition to and independently from the normal Port A I/O functions. The maximum rate at which an edge can be detected is one-half the ∅2 clock rate. The edge detect logic is continuously active. Each edge detect signal is associated with a maskable interrupt.

PA0 Positive Edge Detection

A positive (rising) edge is detectable on PA0. When this edge is detected, the PA0 Positive Edge Detected bit—Bit 6 in the Control Register—is set to Logic 1. When both this bit and the PA0 Interrupt Enable Bit—Bit 3 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA0 Positive Edge Detected bit is cleared by writing to address 089.

PA1 Negative Edge Detection

A negative (falling) edge is detectable on PA1. When this edge is detected, the PA1 Negative Edge Detected bit—Bit 5 of the Control Register—is set to Logic 1. When both this bit and the PA1 Interrupt Enable bit—Bit 2 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA1 Negative Edge Detected bit is cleared by writing to address 08A.

COUNTER/LATCH

The Counter/Latch consists of a 16-bit decrementing Counter and a 16-bit Latch. The Counter is comprised of two 8-bit registers. Address 086 contains the Upper Count (UC) and address 087 contains the Lower Count (LC). The Counter counts either ∅2 clock periods or occurrences of an external event, depending on the selected counter mode. The UC and LC can be read at any time without affecting counter operation.

The Latch contains the Counter preset value. The Latch consists of two 8-bit registers. Address 084 contains the Upper Latch (UL) and address 085 contains the lower latch (LL). The 16-bit Latch can hold a count from 0 to 65,535. The Latch can be accessed as two write-only memory locations.

The Latch registers can be loaded at any time by storing into UL and LL. The UL can also be loaded by writing into address 088.

The Counter can be preset at any time by writing to address 088. Presetting the Counter in this manner causes the contents of the accumulator to be stored into the UL before the 16-bit value in the Latch (UL and LL) is transferred in the Counter (UC and LC).

The Counter is preset to the Latch value when the Counter overflows. When the counter decrements from 0000, Counter overflow occurs causing the next counter value to be the Latch value, not FFFF.

When the Counter overflows, Counter Overflow bit—Bit 7 of the Control Register—is set to Logic 1. When both this bit and the Counter Interrupt Enable bit—Bit 4 of the Control Register—are set, an $\overline{IRQ}$ interrupt request is generated. The Counter Overflow bit in the Control Register can be examined in an $\overline{IRQ}$ interrupt service routine to determine that the $\overline{IRQ}$ was generated by Counter overflow.

The Counter Overflow bit is cleared when the LC is read or Counter preset is performed by writing into address 088.

COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC 1	CMC 0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are ∅2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In this mode the Counter is free running and decrements at the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line is held in the high state.

Pulse Generator (Mode 1)

In this mode the Counter is free running and decrements at the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line toggles from one state to the other when Counter overflow occurs. Writing to address 088 will also toggle the CNTR line.

A symmetric or asymmetic output waveform can be generated on the CNTR line in this mode. A one-shot waveform can easily be generated by changing from Mode 1 to Mode 0 after only one occurrence of the output toggle condition.

Event Counter (Mode 2)

In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR. The maximum rate at which this edge can be detected is one-half the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

Pulse Width Measurement (Mode 3)

This mode allows the accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the ∅2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state. If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high state.

RESET CONSIDERATIONS

The occurrence of $\overline{RES}$ going from low to high causes initialization of various conditions in the 6500/1. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (Logic 1) state. All bits of the Control Register are reset to Logic 0, causing the Interval Timer Mode (Mode 0) to be selected and all interrupt enabled bits to be cleared. Neither the Latch nor the Counter registers are initialized by $\overline{RES}$. The Interrupt Disable bit in the CPU Processor Status Register is set and the program starts execution at the address contained in the Reset Vector location.

TEST LOGIC

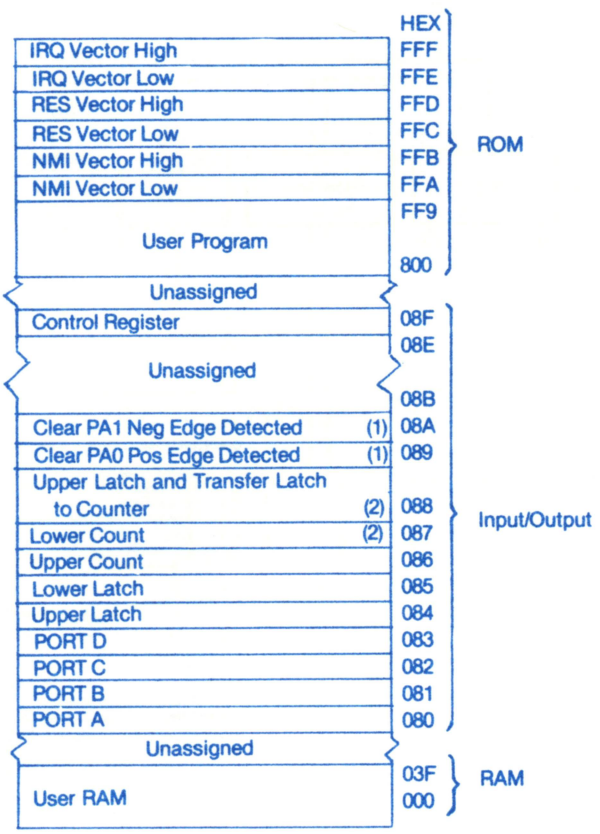
Special test logic provides a method for thoroughly testing the 6500/1. Applying a + 10V signal to the $\overline{RES}$ line places the 6500/1 in the test mode. While in this mode, all memory fetches are made from Port PC. External test equipment can use this feature to test internal CPU logic and I/O. A program can be loaded into RAM allowing the contents of the instruction ROM to be dumped to any port for external verification.

All 6500/1 microcomputers are tested by MOS Technology using this feature.

MEMORY ADDRESSABLE I/O

The I/O ports, registers, and commands are treated as memory and are assigned specific addresses. See the system memory map for the addresses. This I/O technique allows the full set of CPU instructions to be used in the generation and sampling of I/O commands and data. When an instruction is executed with an I/O address and appropriate R/W state, the corresponding I/O function is performed.

SYSTEM MEMORY MAP



Notes:

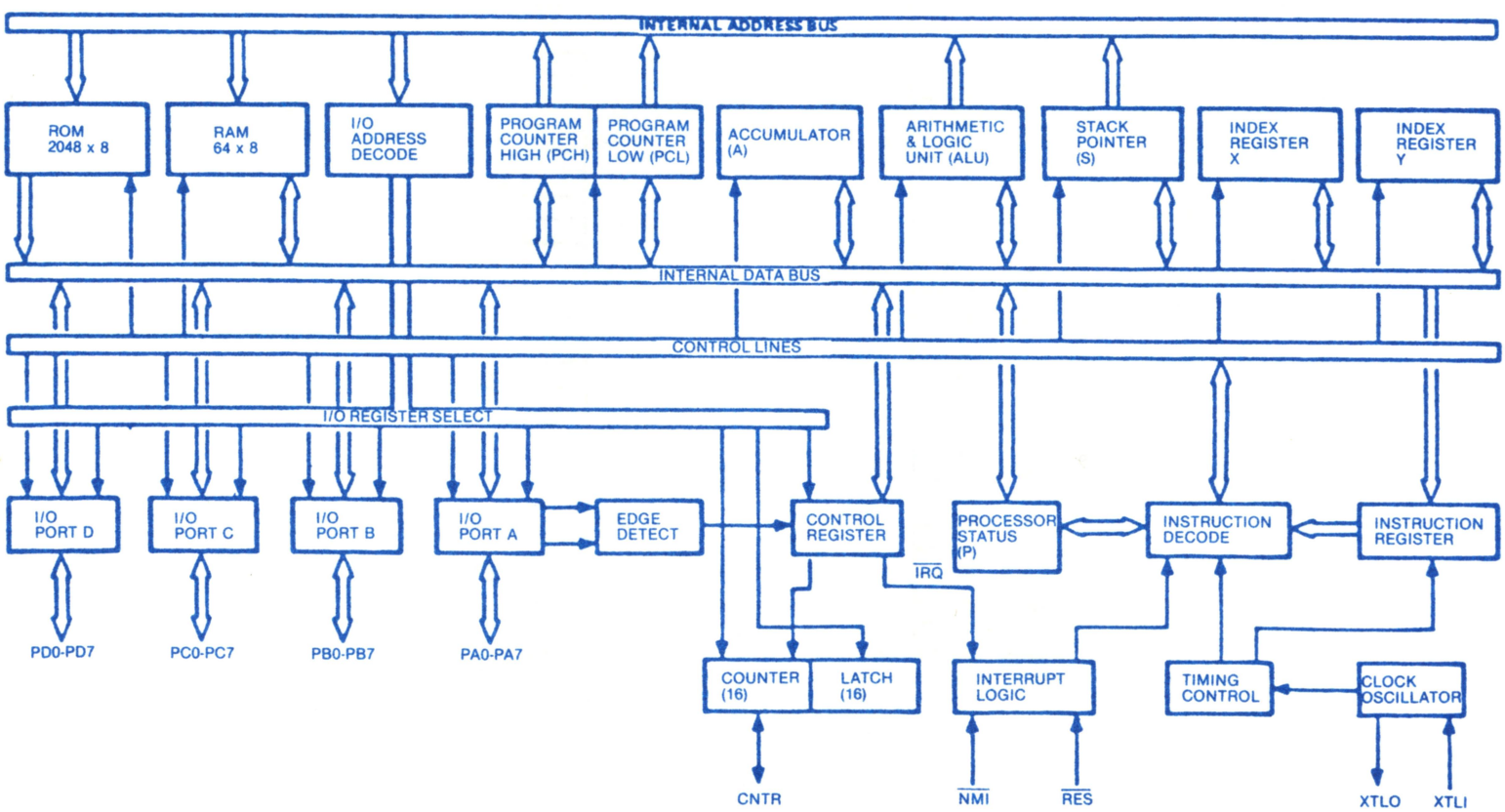
(1) I/O command only; i.e., no stored data.

(2) Clears Counter Overflow—Bit 7 in Control Register.

INSTRUCTION SET—ALPHABETIC SEQUENCE

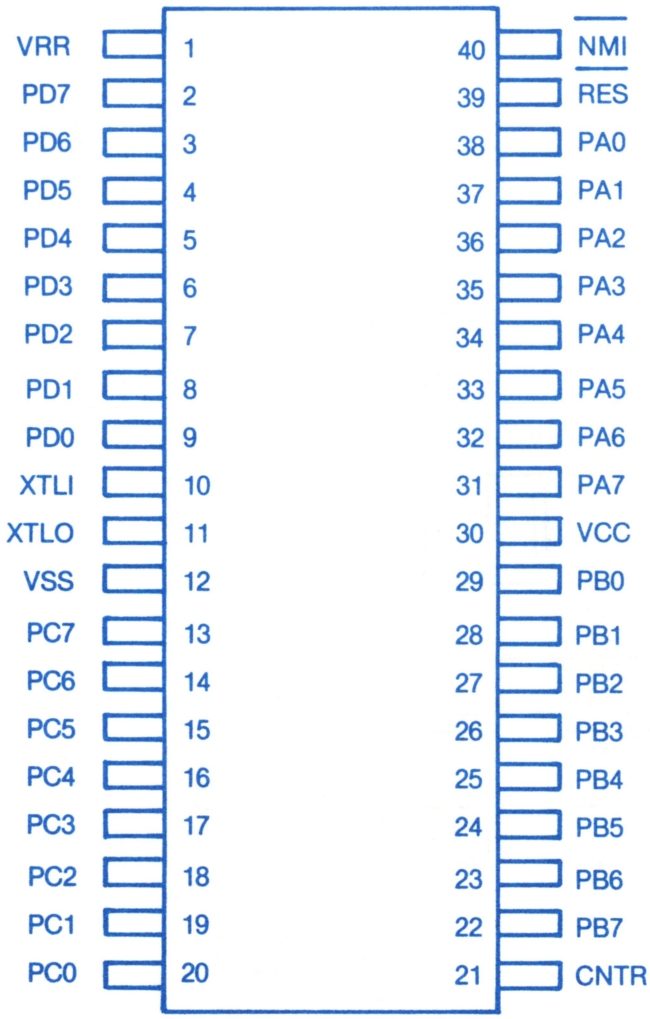
ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEO	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

6500/1 Block Diagram



SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NO.	DESCRIPTION
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network output from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the 6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized. +10V input enables the test mode.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8 bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to +5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.



Pin Configuration

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to $+127$ bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE N	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE N	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE N	ZERO PAGE #	ACCUM OP	ACCUM N	ACCUM #	IMPLIED OP	IMPLIED N	IMPLIED #	(IND,X) OP	(IND,X) N	(IND,X) #	(IND),Y OP	(IND),Y N	(IND),Y #	Z PAGE,X OP	Z PAGE,X N	Z PAGE,X #	ABS,X OP	ABS,X N	ABS,X #	ABS,Y OP	ABS,Y N	ABS,Y #	RELATIVE OP	RELATIVE N	RELATIVE #	(IND) OP	(IND) N	(IND) #	Z PAGE,Y OP	Z PAGE,Y N	Z PAGE,Y #	CONDITION CODES N	Z	C	I	D	V
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	–	–	✓
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	–	–	–	–
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	–	–	–
BCC	BRANCH ON C=0 (2)																															90	2	2							–	–	–	–	–	–
BCS	BRANCH ON C=1 (2)																															B0	2	2							–	–	–	–	–	–
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							–	–	–	–	–	–
BIT	A ∧ M				2C	4	3	24	3	2																															M7	✓	–	–	–	M6
BMI	BRANCH ON N=1 (2)																															30	2	2							–	–	–	–	–	–
BNE	BRANCH ON Z=0 (2)																															D0	2	2							–	–	–	–	–	–
BPL	BRANCH ON N=0 (2)																															10	2	2							–	–	–	–	–	–
BRK	(See Fig. 1)													00	7	1																									–	–	–	–	–	–
BVC	BRANCH ON V=0 (2)																															50	2	2							–	–	–	–	–	–
BVS	BRANCH ON V=1 (2)																															70	2	2							–	–	–	–	–	–
CLC	0 → C													18	2	1																									–	–	0	–	–	–
CLD	0 → D													D8	2	1																									–	–	–	–	0	–
CLI	0 → I													58	2	1																									–	–	–	0	–	–
CLV	0 → V													B8	2	1																									–	–	–	–	–	0
CMP	A-M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	–	–	–
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	–	–	–
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	–	–	–
DEC	M-1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	–	–	–	–
DEX	X-1 → X													CA	2	1																									✓	✓	–	–	–	–
DEY	Y-1 → Y													88	2	1																									✓	✓	–	–	–	–
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	–	–	–	–
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	–	–	–	–
INX	X + 1 → X													E8	2	1																									✓	✓	–	–	–	–
INY	Y + 1 → Y													C8	2	1																									✓	✓	–	–	–	–
JMP	JUMP TO NEW LOC				4C	3	3																													6C	5	3				–	–	–	–
JSR	(See Fig. 2) JUMP SUB				20	6	3																																			–	–	–	–	–	–
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	–	–	–	–

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE N	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE N	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE N	ZERO PAGE #	ACCUM OP	ACCUM N	ACCUM #	IMPLIED OP	IMPLIED N	IMPLIED #	(IND,X) OP	(IND,X) N	(IND,X) #	(IND),Y OP	(IND),Y N	(IND),Y #	Z PAGE,X OP	Z PAGE,X N	Z PAGE,X #	ABS,X OP	ABS,X N	ABS,X #	ABS,Y OP	ABS,Y N	ABS,Y #	RELATIVE OP	RELATIVE N	RELATIVE #	(IND) OP	(IND) N	(IND) #	Z PAGE,Y OP	Z PAGE,Y N	Z PAGE,Y #	CONDITION CODES N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							86	4	2	✓	✓	–	–	–	–
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													✓	✓	–	–	–	–
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	–	–	–
NOP	NO OPERATION													EA	2	1																									–	–	–	–	–	–
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	–	–	–	–
PHA	A → Ms S-1 → S													48	3	1																									–	–	–	–	–	–
PHP	P → Ms S-1 → S													08	3	1																									–	–	–	–	–	–
PLA	S+1 → S Ms → A													68	4	1																									✓	✓	–	–	–	–
PLP	S+1 → S Ms → P													28	4	1																									(RESTORED)					
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	–	–	–
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	–	–	–
RTI	(See Fig. 1) RTRN INT													40	6	1																									(RESTORED)					
RTS	(See Fig. 2) RTRN SUB													60	6	1																									–	–	–	–	–	–
SBC	A-M-C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)	–	–	✓
SEC	1 → C													38	2	1																									–	–	1	–	–	–
SED	1 → D													F8	2	1																									–	–	–	–	1	–
SEI	1 → I													78	2	1																									–	–	–	1	–	–
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										–	–	–	–	–	–
STX	X → M				8E	4	3	86	3	2																													96	4	2	–	–	–	–	–	–
STY	Y → M				8C	4	3	84	3	2													94	4	2																–	–	–	–	–	–
TAX	A → X													AA	2	1																									✓	✓	–	–	–	–
TAY	A → Y													A8	2	1																									✓	✓	–	–	–	–
TSX	S → X													BA	2	1																									✓	✓	–	–	–	–
TXA	X → A													8A	2	1																									✓	✓	–	–	–	–
TXS	X → S													9A	2	1																									–	–	–	–	–	–
TYA	Y → A													98	2	1																									✓	✓	–	–	–	–

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT - BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
- SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
– NOT MODIFIED
M7 MEMORY BIT 7
M6 MEMORY BIT 6
N NO CYCLES
NO BYTES

Note: MOS Technology cannot assume liability for the use of undefined OP Codes

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Static D.C. Characteristics (V_{CC} = 5V ±5%, T_A = 0° −70° C)

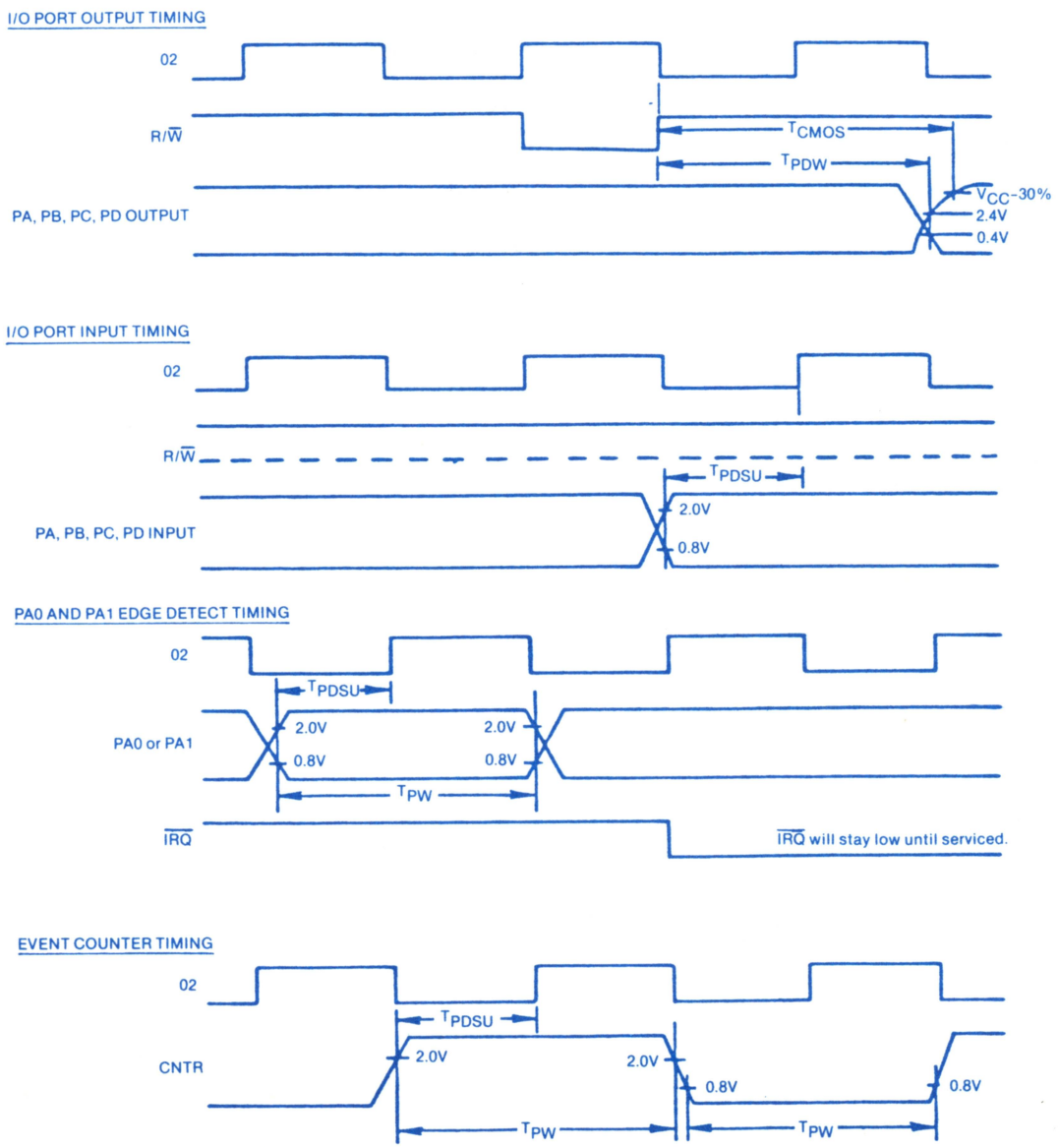
Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D	—	500	—	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}	—	10	—	mAdc
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current					
V_{in} = 0 to 5.0 Vdc	I_{IN}	—	±1.0	±2.5	μAdc
RES, NMI		—	±1.0	—	μAdc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	−0.3	—	+0.8	Vdc
Input Low Current					
(V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage					
(V_{CC} = min, I_{Load} = −100 μAdc)	V_{OH}	−2.4	—	—	Vdc
Output High Voltage	V_{CMOS}	V_{CC} − 30%	—	—	Vdc
(V_{CC} = min)					
Output Low Voltage					
(V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing)					
(V_{OH} = 2.4 Vdc)	I_{OH}	−100	—	—	μAdc
Output Low Current (Sinking)					
(V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance					
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PA, PB, PC, PD, CNTR	C_{in}	—	—	10	pF
XTLI, XTLO		—	—	50	pF
Output Capacitance					
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	—	10	pF
I/O Port Resistance	R_L	3.0	6.0	11.5	KΩ
PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR					

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0	—	0.5	—	μsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0	—	1.0	—	μsec
Peripheral Data Setup Time	T_{PDSU}	400	—	200	—	nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0	—	0.5	—	μsec

TIMING CHARACTERISTICS



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ORDER QUESTIONNAIRE

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information. Due to device design, chip option information must be implemented coincident with ROM program.

Code Name (if any) _____ Customer Part Number _____

Special Instructions _____ Customer P.O. Number _____

_____ Date _____

CUSTOMER:

Company _____

Division _____

Address _____

City _____ State _____ Zip _____

Technical Contact _____ Tel. (____) _____

Production Authorization _____ Date _____

Authorized Signature

Part Marking _____

Specify (Optional — Maximum 12 Characters or Spaces)

External Frequency Reference is: _____ (Specify "C" or "R")

C = Crystal or Clock
R = RC Network

Check desired Pull-Up Option:

I/O Port A	Leave Internal Pull-Ups* _____	Delete Internal Pull-Ups	_____
I/O Port B	Leave Internal Pull-Ups* _____	Delete Internal Pull-Ups	_____
I/O Port C	Leave Internal Pull-Ups* _____	Delete Internal Pull-Ups	_____
I/O Port D	Leave Internal Pull-Ups* _____	Delete Internal Pull-Ups	_____
CNTR	Leave Internal Pull-Up* _____	Delete Internal Pull-Up	_____

*Same as R6500/1E Emulator Device

ROM Start and Stop Address in Submitted Media (Tapes, Cards):

ROM Data Start Address is: _____ _____ _____ (three hexadecimal digits) (min = 800)

ROM Date Stop Address is: _____ _____ _____ (three hexadecimal digits) (must be = FFF)

Note: FFA — FFF must contain NMI, RES and IRQ vectors, respectively.

Note: All addresses and related bit patterns must be completely defined.

Input and Verify Media: ☐ Paper Tape ☐ Card Deck ☐ Eprom ☐ Other _____

SPECIFY

Date Format: ☐ INTEL HEX ☐ M.O.S. HEX ☐ Other _____

SPECIFY

Verification: ☐ Hold ☐ Not Required ☐ Released _____

DATE

Note 1: Positive true logic: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 2: The above program data formats are the only acceptable formats for ROMS. Other formats may be possible but only with marketing evaluation and clearance.

Note 3: Only 2716 (except TI), 2516, 2732 Proms or multiples of same are acceptable as Prom Program Inputs. Two copies of each Prom are preferred.

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